

What is claimed:

Sub A  
1 1. A method for manufacturing a semiconductor device having a trench element  
2 isolation region including a trench and a trench insulating layer that fills the trench, the  
3 method comprising the steps of:

4 (A) forming a polishing stopper layer over a substrate, the polishing stopper layer  
5 having a predetermined pattern for a chemical-mechanical polishing;

6 (B) removing a part of the substrate using a mask layer including at least the  
7 polishing stopper layer as a mask to form a trench;

8 (C) forming a trench oxide film over a surface of the substrate that forms the trench;

9 (D) forming an insulating layer that fills the trench over an entire surface of the  
10 substrate;

11 (E) polishing the insulating layer by a chemical-mechanical polishing;

12 (F) removing the polishing stopper layer; and

13 (G) etching a part of the insulating layer to form a trench insulating layer,

14 wherein the method further includes the step (a) of forming an etching stopper layer  
15 for the trench oxide film over at least a portion of the trench oxide film, and wherein, in the  
16 step (G), the etching stopper layer is more resistant to the etching than insulating layer.

1 2. A method for manufacturing a semiconductor device according to claim 1,  
2 wherein, in the step (G), a selective etching ratio of the insulating layer with respect to the  
3 etching stopper layer is 10 or greater.

1 3. A method for manufacturing a semiconductor device according to claim 1,  
2 wherein the etching stopper layer is formed to cover a side surface of the trench oxide film.

sub B  
1 4. A method for manufacturing a semiconductor device according to claim 1,  
2 wherein the etching stopper layer is a silicon nitride layer.

1 ~~5.~~ <sup>5.</sup> A method for manufacturing a semiconductor device according claim 4,  
2 wherein the silicon nitride layer has a thickness of 10 – 50 nm.

1 6. A method for manufacturing a semiconductor device according to claim 1,  
2 wherein the etching stopper layer is a non-monocrystal silicon layer.

1 7. A method for manufacturing a semiconductor device according claim 6,  
2 wherein the non-monocrystal silicon layer is selected from the group consisting of a  
3 polycrystal silicon layer, an amorphous silicon layer or a multiple layer having a polycrystal  
4 silicon layer and an amorphous silicon layer.

1 8. A method for manufacturing a semiconductor device according claim 6,  
2 wherein the non-monocrystal silicon layer has a thickness of 20 – 50 nm.

1 9. A method for manufacturing a semiconductor device according to claim 6,  
2 further comprising, after the step (G), the step (b) of thermally oxidizing a portion of the  
3 non-monocrystal layer that protrudes from the surface of the substrate in an element forming  
4 region to form a silicon oxide film.

1 10. A method for manufacturing a semiconductor device according claim 9,  
2 wherein the silicon oxide film is removed at the same time as the step (G).

1 11. A semiconductor device comprising trench element isolation regions,  
2 wherein at least one of the trench element isolation regions includes a trench oxide film  
3 formed on a surface of a substrate that forms a trench, and a trench insulating layer formed  
4 in the trench, wherein an etching stopper layer is formed such that a surface of the trench  
5 oxide film on a side wherein the trench insulating layer is formed is not exposed.

1           12.    A semiconductor device comprising trench element isolation regions,  
2 wherein at least one of the trench element isolation regions comprises:  
3           a trench oxide film formed on a surface of a substrate that forms a trench,  
4           a trench insulating layer formed in the trench, and  
5           an etching stopper layer formed between the trench oxide film and the trench  
6 insulating layer.

1           13.    A semiconductor device according to claim 12, wherein the etching stopper  
2 layer is formed from a material having a selective etching ratio of the insulating layer to the  
3 etching stopper layer of at least ten (10) when an etchant including hydrofluoric acid is used.

1           14.    A semiconductor device according to claim 12, wherein the etching stopper  
2 layer is formed on a surface of the trench oxide film.

1           15.    A semiconductor device according to claim 12, wherein the etching stopper  
2 layer comprises a silicon nitride layer.

1           16.    A semiconductor device according to claim 12, wherein the etching stopper  
2 layer is a silicon nitride layer having a thickness of 10 – 50 nm.

1           17.    A semiconductor device according to claim 12, wherein the etching stopper  
2 layer comprises a non-monocrystal silicon layer.

1           18.    A semiconductor device according to claim 12, wherein the etching stopper  
2 layer is a non-monocrystal silicon layer having a thickness of 20 – 50 nm.

25. A semiconductor device according to claim 24, wherein the non-monocrystal silicon layer is selected from the group consisting of a polycrystal silicon layer, an amorphous silicon layer or a multiple layer having a polycrystal silicon layer and an amorphous silicon layer.

- 1           26.    A method for manufacturing a semiconductor device, comprising:  
2           forming a trench comprising a lower surface and two side surfaces in a substrate  
3   comprising silicon;  
4           forming a trench oxide layer on the lower surface and side surfaces;  
5           forming an etch stop layer in direct contact with the trench oxide layer on the lower  
6   surface and side surfaces;  
7           filling the trench with an insulating layer directly contacting the etch stop layer,  
8   wherein the insulating layer overfills the trench and extends above the trench as defined by  
9   the two side surfaces; and  
10          etching the insulating layer using an etchant that selectively etches the etch stop layer  
11   at a rate that is slower than that of the insulating layer.

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